REMARKS

Claim 20 has been amended to properly recite the structure of claim 19 from which it depends. Claims 1-22 remain for consideration in this application.

Rejections Under 35 U.S.C. § 102

Claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Abedifard (U. S. Patent No. 6,366,524). Applicant traverses the rejections, and submits that Abedifard does not contain each and every element of the claims, as is required to support a rejection under 35 U.S.C. § 102(b). Abedifard is directed generally to working with delays in decoding provided addresses to accommodate a complex memory structure. In contrast, the present application is directed generally to configuration of the number of banks in a memory, and the associated structure and methods to accomplish that.

With reference to the entire pending claim set and the rejections thereof, Applicant submits that nowhere in Abedifard is any mention made at all of configuring the number of banks in a memory. In fact, nowhere in Abedifard is there made any mention of any memory that does not have four banks. Figure 1, which has been asserted by the Office Action as showing wither four or eight banks, clearly and unambiguously shows four banks, namely banks 104, 106, 108, and 110. There is no mention of reconfiguring the number of banks, and there is certainly no mention of the same physical structure being configurable into a different arrangement of banks, as is the subject generally of the pending claims. Further, the assertion that status register 134 is a "mode register" that performs the functions of the mode register identified and recited in the present claims is wholly unsupported by the specification and figures of Abedifard. In fact, the only mention of the status register 134 in Abedifard is at column 5, lines 18-19, which state "A status register 134 and an identification register 136 can also be provided **to output data**." (emphasis added). This function of outputting data has nothing to do with the mode register of the pending claims that specifically is recited for configuring the banks.

Specifically, claim 1 recites "address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register." This is neither taught nor disclosed in Abedifard. The status register 134 of Abedifard is for outputting data. There is no mention of any state of status register 134 being used to configure the addressable banks as is

recited in claim 1. Further, Abedifard contains no teaching or disclosure of configuring the addressable banks in any way. Applicant respectfully submits that claim 1 is allowable. Claims 2-3 depend from and further define patentably distinct claim 1 and are also believed allowable.

Claim 4 recites "address circuitry coupled to the mode register to configure the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array." Once again, this is neither taught nor disclosed in Abedifard. The status register 134 of Abedifard performs no function of defining a number of banks or of configuring the array as is recited in the claim. Applicant respectfully submits that claim 4 is allowable. Claims 5-8 depend from and further define patentably distinct claim 4 and are also believed allowable.

Claim 9 recites "address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored in the mode register." Again, this is neither taught nor disclosed in Abedifard. The status register 134 of Abedifard performs no function of defining a number of banks or of configuring the array as is recited in the claim. Applicant respectfully submits that claim 9 is allowable. Claims 10-11 depend from and further define patentably distinct claim 9 and are also believed allowable.

Claim 19 recites "logic circuitry coupled to the at least one external input connection" and "address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to the logic circuitry." No logic circuitry configured as is recited in the claim to route the addresses received at address signal circuitry is taught or disclosed in Abedifard. As such, Applicant respectfully submits that claim 19 is allowable. Claims 20-21 depend from and further define patentably distinct claim 19 and are also believed allowable.

Claim 12 recites "adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array" and claim 16 recites "adjusting address circuitry of the memory device in response to the programmed mode register, wherein the address circuitry configures a number of addressable banks of a memory cell array using the bank count data." As has been

described and discussed above, this is neither taught nor disclosed in Abedifard. Specifically, Abedifard does not tech adjusting address circuitry in response to a programmed mode register as is recited in claim 12, nor does Abedifard teach that the mode register data contains bank count data as is recited in claim 16. As such, Applicant respectfully submits that claims 12 and 16 are allowable. Claims 13-15 and 17-18 depend from and further define one of patentably distinct claims 12 or 16 and are also believed allowable.

CONCLUSION

In view of the above remarks, the Applicant respectfully submits that all claims are now in condition for allowance and requests reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicant's attorney to discuss any questions that may remain with respect to the present application. No new matter has been entered with this amendment and no additional fee is required.

Respectfully submitted,

Christopher S. Johnson

By his Representatives,

Leffert Jay & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009
(612) 312-2203

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By Daniel J Polglaze

Daniel J. Polglaze
Reg. No. 39,801